1U 2000W PSU Engineering Reference Specifications

Model : R18-2K0P1XC
MFG No : TBD
UP/N : TBD

Revision History

Revision	Revision Description	Date
A	New release	2021/02/05

EE Engineer	ME Engineer	Safety	R&D Leader
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1. SCOPE

The specification defines the performance characteristics for the 2000W Common Redundant Power Supply (CRPS) supporting server systems with a 12V2 main output and 12VSB standby output.

2. Mechanical overview

The physical size of the power supply enclosure is 39/40(H)mm x 73.5(W)mm x 185(L)mm. The power supply contains a single rotor fan (40x40x28mm). The power supply has a card edge output that interfaces with a card edge connector in the system. The AC plugs into the external face of the power supply directly. All for detail please refer to mechanical outline drawing.

2.1 DC output connector

The power supply card edge pin-assignment defines in the below table and mating connector is AMPHENOL GPCP145000111HR.

Pin	Name	Pin	Name
A1	GND	B1	GND
A2	GND	B2	GND
A3	GND	B3	GND
A4	GND	B4	GND
A5	GND	B5	GND
A6	GND	B6	GND
A7	GND	B7	GND
A8	GND	B8	GND
A9	GND	B9	GND
A10	+12V2	B10	+12V2
A11	+12V2	B11	+12V2
A12	+12V2	B12	+12V2
A13	+12V2	B13	+12V2
A14	+12V2	B14	+12V2
A15	+12V2	B15	+12V2
A16	+12V2	B16	+12V2
A17	+12V2	B17	+12V2
A18	+12V2	B18	+12V2
A19	SDA	B19	A0 (SMBus address)
A20	SCL	B20	A1 (SMBus address)
A21	PSON	B21	12VSB
A22	SMBALERT#	B22	CR_Bus
A23	RS-	B23	ISHARE
A24	RS+	B24	PRESENT
A25	PWOK	B25	VIN_GOOD

Note: There is an impedance from 20K to 50K Ω on B22 “CR_Bus” pin and an impedance 100 ohm on B24 “PRESENT” connect to GND, system must consider impedance matching.

2.2 Handle retention

The power supply shall have a handle to assist extraction. The module shall be able to be inserted and extracted without the assistance of tools. The power supply shall have a latch which retains the power supply into the system and prevents the power supply from being inserted or extracted from the system when the AC power cord is pulled into the power supply.

2.3 LED marking and identification

The power supply shall use a bi-color LED; Amber & Green. Below are table showing the LED states for each power supply operating state and the LED's wavelength characteristics. An example bi-color LED that meets the below characteristics is Kingbright WP59-CN99.

Table 1 LED characteristics

	Min λd Wavelength	**Nominal λd Wavelength**	**Max λd Wavelength**	**Units**
Green	562	565	568	nm
Amber	607	610	613	nm

Table 2 LED indicator status

Power Supply Condition	**LED State**
Output ON and OK	GREEN
No AC power to all power supplies	OFF
PSU standby state AC present / Only 12VSB on	1Hz Blink GREEN
Power supply is cold standby state or always standby state as defined in the Cold Redundancy section of the CRPS Common Requirements Specification	1Hz Blink GREEN
AC cord unplugged or AC power lost; with a second power supply in parallel still with AC input power.	OFF
Power supply critical event causing a shutdown; failure, over current, short circuit, over voltage, fan failure, over temperature, input over voltage	AMBER
Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan.	1Hz Blink Amber
Power supply FW updating	2Hz Blink GREEN

2.4 Acoustic requirements

The power supply shall incorporate variable speed fan(s). The declared sound power levels (LwAd) of the power supply must meet the requirements shown in the table below. Sound power must be measured according to ECMA 74 (www.ecma-international.org) and reported according to ISO 9296/ISO7779.

Table 3 Sound Power level requirement

Inlet Temperature Condition	**% of Maximum Loading Condition**	**Sound Power (BA)**
50°C	100%	8.6
50°C	50%	7.6
50°C	20%	5.8

3. AC INPUT REQUIREMENTS

3.1 Power factor and iTHD

The power supply must meet the power factor and current iTHD requirements are stated below. These requirements are within the Energy Star® Program Requirements for Computer Servers.

Table 4 Power Factor Requirements

Output power	**10% load**	**20% load**	**50% load**	**100% load**
Power factor	> 0.9	> 0.96	> 0.98	> 0.99
Input conditions	230VAC & 50Hz / 60Hz			

Table 5 iTHD Requirements

Output power	**10% load**	**20% load**	**50% load**	**100% load**
Current iTHD	< 20%	< 10%	≤8%	≤5%
Input conditions	230VAC & 50Hz / 60Hz			

3.2 Leakage current maximum

Maximum input leakage current at 230V AC, 50Hz shall not exceed 0.5mA.

3.3 AC Inlet connector

The AC input connector shall be an *IEC 320 C-14* power inlet. This inlet is rated for 10A / 250VAC.

3.4 Input voltage / current specification

The power supply must operate within all specified limits over the following input voltage range. Harmonic distortion of up to 10% of the rated line voltage must not cause the power supply to go out of specified limits. Application of an input voltage below 85VAC shall not cause damage to the power supply, including a blown fuse.

Table 6 Input voltage / current specification

PARAMETER	**MIN**	**Nominal**	**MAX**	**Start up VAC**	**Power Off VAC**
Line Voltage (110V_{rms})	90V_{rms}	100-127 V_{rms}	140V_{rms}	85VAC +/-2VAC	80VAC +/-2VAC
Line Voltage (220V_{rms})	180V_{rms}	200-240 V_{rms}	264V_{rms}		
Frequency	47 Hz	50-60Hz	63 Hz		
Line Voltage (240V_{DC})	164V_{DC}	240V_{DC}	300V_{DC}		
Line RMS current load			230V_{rms} 10A 100 V_{rms} 13A 240 V_{DC} 9.3A		

3.5 AC line isolation requirement

Parameter	Setting
Voltage	2121Vdc Minimum
Trip current sensitivity	600 Microamperes Maximum
Voltage ramp time	500V/Second ramp Minimum
Dwell time	1 Second Minimum
Breakdown arc detection	10 Microseconds Maximum

3.6 AC line dropout / holdup

An AC line dropout is defined to be when the AC input drops to 0VAC at any phase of the AC line for any length of time. During an AC dropout the power supply must meet dynamic voltage regulation requirements. An AC line dropout of any duration shall not cause tripping of control signals or protection circuits other than the SMBAlert# signal. If the AC dropout lasts longer than the holdup time the power supply should recover and meet all turn on requirements. The power supply shall meet the AC dropout requirement over rated AC voltages and frequencies. A dropout of the AC line for any duration shall not cause damage to the power supply.

Table 7 AC Holdup / Dropout

Loading during AC dropout / holdup	Holdup time / Dropout duration
0% to 70% of rated load	10msec

3.6.1 AC line 12VSB holdup

The 12VSB output voltage should stay in regulation under its full load (static or dynamic) during an AC dropout of **70ms min** (=12VSB holdup time) whether the power supply is in ON or OFF state (PSON asserted or de-asserted).

3.7 AC line fuse

The power supply shall have one line fused in the single line fuse on the line (Hot) wire of the AC input. The line fusing shall be acceptable for all safety agency requirements. The input fuse shall be a fast blow type. AC inrush current shall not cause the AC line fuse to blow under any conditions. All protection circuits in the power supply shall not cause the AC fuse to blow unless a component in the power supply has failed. This includes DC output load short conditions.

3.8 AC inrush

Cold Start：Any additional inrush current surges or spikes in the form of AC cycles or multiple AC must not exceed 35A peak.The inrush spike (<1mS) due to the EMI filter capacitors can be ignored.

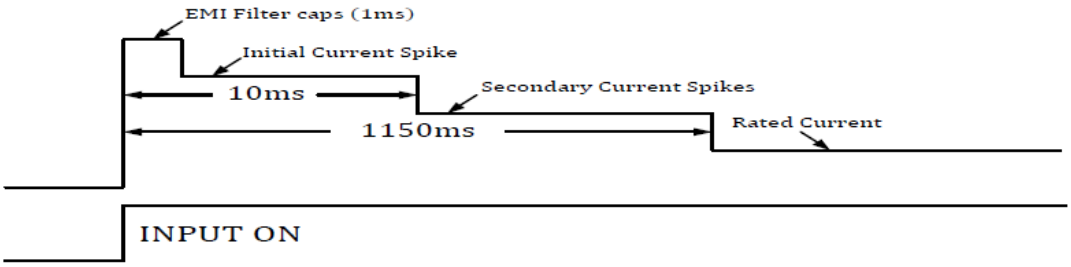
Warm start：Power supply shall not damage and the peak current shall be less than the rating of its critical components including input fuse, bulk rectifier and surge limits devices.

The Cold start inrush current during 1~1150ms,peak current should be less than spec in the Table 8.

Table 8 Cold start inrush current

Output Power	Cold Inrush should less than
2000W	<=35A

The power Supply must meet “cold start inrush current” requirements for any combination of input voltages and frequencies and over the specified temperature range.



3.9 AC line transient specification

AC line transient conditions shall be defined as “sag” and “surge” conditions. “Sag” conditions are also commonly referred to as “brownout”, these conditions will be defined as the AC line voltage dropping below nominal voltage conditions. “Surge” will be defined to refer to conditions when the AC line voltage rises above nominal voltage.

The power supply shall meet the requirements under the following AC line sag and surge conditions.

Table 9 AC Line Sag Transient Performance

AC Line Sag (10sec interval between each sagging)				
Duration	Sag	Operating AC Voltage	Line Frequency	Performance Criteria
0 to 1/2 AC cycle	95%	Nominal AC Voltage ranges	50/60Hz	No loss of function or performance
> 1 AC cycle	>30%	Nominal AC Voltage ranges	50/60Hz	Loss of function acceptable, self-recoverable

Table 10 AC Line Surge Transient Performance

AC Line Surge				
Duration	Surge	Operating AC Voltage	Line Frequency	Performance Criteria
Continuous	10%	Nominal AC Voltages	50/60Hz	No loss of function or performance
0 to ½ AC cycle	30%	Mid-point of nominal AC Voltages	50/60Hz	No loss of function or performance

3.10 Susceptibility requirements

The power supply shall meet the following electrical immunity requirements when connected to a cage with an external EMI filter which meets the criteria defined in the SSI document EPS Power Supply Specification. For further information on Intel standards please request a copy of the Intel Environmental Standards Handbook

Table 11 Performance Criteria

Level	Description
A	The apparatus shall continue to operate as intended. No degradation of performance.
B	The apparatus shall continue to operate as intended. No degradation of performance beyond spec limits.
C	Temporary loss of function is allowed provided the function is self-recoverable or can be restored by the operation of the controls.

3.11 Electrostatic Discharge Susceptibility

The power supply shall comply with the limits defined in EN 55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-2: Edition 1.2: 2001-04 test standard and performance criteria B defined in Annex B of CISPR 24.

3.12 Fast Transient/Burst

The power supply shall comply with the limits defined in EN55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-4: Second edition: 2004-07 test standard and performance criteria B defined in Annex B of CISPR 24.

3.13 Radiated Immunity

The power supply shall comply with the limits defined in EN55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-3: Edition 2.1: 2002-09 test standard and performance criteria A defined in Annex B of CISPR 24.

3.14 Surge Immunity

The power supply shall be tested with the system for immunity to AC Unidirectional wave; 2kV line to ground and 1kV line to line, per EN 55024: 1998/A1: 2001/A2: 2003, EN 61000-4-5: Edition .1:2001-04 .

The pass criteria include: No unsafe operation is allowed under any condition; all power supply output voltage levels to stay within proper spec levels; No change in operating state or loss of data during and after the test profile; No component damage under any condition.

The power supply shall comply with the limits defined in EN55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-5: Edition 1.1:2001-04 test standard and performance criteria B defined in Annex B of CISPR 24.

3.15 Voltage Interruptions

The power supply shall comply with the limits defined in EN55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-11: Second Edition: 2004-03 test standard and performance criteria C defined in Annex B of CISPR 24.

4. Efficiency

The following table provides the required minimum efficiency levels at various loading conditions. These are provided at different load levels; 100%, 50%, 20% and 10%. Output shall be load according to the proportional loading method defined by 80 Plus in Generalized Internal Power Supply Efficiency Testing Protocol Rev 6.7. In these testing requirements the power supply is tested at 230VAC/60/50 Hz and 240VDC input and does not include the losses of the PSU fan.

Table 12 Efficiency Requirement

Loading	**100% of maximum**	**50% of maximum**	**20% of maximum**	**10% of maximum**
Platinum efficiency	91%	94%	93%	90%

5. DC Output Specification

5.1 Output Power / Currents

The following tables define the minimum power and current ratings. The power supply must meet both static and dynamic voltage regulation requirements for all conditions. When input voltage and loading change (in the different range) at the same time that PSU can allow shut down and restart, but cannot damage. For any heavy load condition, when applied unsuitable AC range might cause an input over power protection event, thus PSU shut down but cannot damage.

Table 13 Minimum Load Ratings

Parameter	Input range	Min. Current	Max. Current
+12V2	$220V_{rms}$ - $264V_{rms}$ / $220V_{DC}$ - $300V_{DC}$	1A	161.5A
	$200V_{rms}$ - $219V_{rms}$ / $200V_{DC}$ - $219V_{DC}$	1A	145.1A
	$180V_{rms}$ - $199V_{rms}$ / $164V_{DC}$ - $199V_{DC}$	1A	128.7A
	$100V_{rms}$ - $127V_{rms}$	1A	79.5A
	$90V_{rms}$ - $99V_{rms}$	1A	71.3A
12VSB	$90V_{rms}$ - $264V_{rms}$ / $164V_{DC}$ - $300V_{DC}$	0.1A	2.5A

5.2 Standby Output

The 12VSB output shall be present when an AC input greater than the power supply turn on voltage is applied.

5.3 Voltage regulation

The power supply output voltages must stay within the following voltage limits when operating at steady state and dynamic loading conditions. These limits include the peak-peak ripple/noise. These shall be measured at the output connectors.

Table 14 Voltage Regulation Limits

PARAMETER	TOLERANCE	MIN	NOM	MAX	UNITS
+12V2	- 5% / +5%	+11.59	+12.20	+12.81	V_{rms}
12VSB	- 5% / +5%	+11.40	+12.00	+12.60	V_{rms}

5.4 Dynamic loading

The output voltages shall remain within limits specified for the step loading and capacitive loading specified in the table below. The load transient repetition rate shall be tested between 50Hz and 5kHz at duty cycles ranging from 10%-90%. The load transient repetition rate is only a test specification. The Δ step load may occur anywhere within the MIN load to the MAX load conditions.

Table 15 Dynamic load requirements

Output	Δ Step Load Size	Load Slew Rate	Test capacitive Load
+12V2	50% of max. load	0.5A / μS	3300μF
12VSB	1.0A	0.25A / μS	100μF

Note: For dynamic condition +12V2 min loading is 1A, 12VSB min loading is 0.1A.

5.5 Capacitive loading

The power supply shall be stable and meet all requirements with the following capacitive loading ranges.

Table 16 Capacitive loading conditions

Output	Min.	Max.	Unit
+12V2	3300	25000	μF
12VSB	100	3300	μF

5.6 Overshoot at turn on / turn off

The output voltage overshoot during the turn-on or turn-off of any output, including the Standby output, should be less than 10% above the nominal voltage and will settle into the regulation band within 20ms. There must be a smooth (monotonic) and continuous ramp of each DC output voltage from 10% to 95% of its final set point within the regulation.

The output voltage undershoot during turn-off of any of the output, including the Standby output shall not exceed 0.3V.

5.7 Remote sense

Differential (Single ended) remote sense is to be provided for the designated remote sense outputs. The remote sense must be able to compensate for the defined system output voltage drop over the system output resistance (after the output connector). A differential amplifier is requested for differential remote sense in redundant PSU. It only provides a very low bandwidth adjustment to the PSU output. It is not intended to adjust the output for transients at the load. Transients are handled through sensing inside the PSU not at the remote sense point. The remote sense lines must be protected such that if only the remote sense is connected to the load, if there is a short across the remote sense or if reverse polarity connection, the power supply is not damaged.

5.8 Grounding

The output ground of the pins of the power supply provides the output power return path. The output connector ground pins shall be connected to the safety ground (power supply enclosure). This grounding should be well designed to ensure passing the max allowed Common Mode Noise levels.

The power supply shall be provided with a reliable protective earth ground. All secondary circuits shall be connected to protective earth ground. Resistance of the ground returns to chassis shall not exceed 1.0 mΩ. This path may be used to carry DC current.

5.9 Closed loop stability

The power supply shall be unconditionally stable under all line/load/transient load conditions. A minimum of: 45 degrees phase margin and -10dB-gain margin is required. The power supply manufacturer shall provide proof of the unit's closed-loop stability with local sensing through the submission of Bode plots. Closed-loop stability must be ensured at the maximum and minimum loads as applicable.

5.10 Residual voltage immunity in standby mode

The power supply should be immune to any residual voltage placed on its outputs (Typically a leakage voltage through the system from standby output) up to 500mV. There shall be no additional heat generated, nor stressing of any internal components with this voltage applied to any individual or all outputs simultaneously. It also should not trip the protection circuits during turn on.

The residual voltage at the power supply outputs for no load condition shall not exceed 100mV when AC voltage is applied and the PSON# signal is de-asserted.

5.11 Zero load stability requirements

When the power subsystem operates in a no load condition, it does not need to meet the output regulation specification, but it must operate without any tripping of over-voltage or other fault circuitry. When the power subsystem is subsequently loaded, it must begin to regulate and source current without fault.

5.12 Hot swap requirements

Hot swapping a power supply is the process of inserting and extracting a power supply from an operating power system. During this process the output voltages shall remain within the limits with the capacitive load specified. The hot swap test must be conducted when the system is operating under static, dynamic, and zero loading conditions. The power supply shall use a latching mechanism to prevent insertion and extraction of the power supply when the AC power cord is inserted into the power supply.

5.13 Force load sharing

The +12V2 output will have active load sharing. The output will share within 5% at full load. The failure of a power supply should not affect the load sharing or output voltages of the other supplies still operating. The supplies must be able to load share in parallel and operate in a hot-swap / redundant 1+1 configurations. The 12VSB output is not required to actively share current between power supplies (passive sharing). The 12VSB output of the power supplies are connected together in the system so that a failure or hot swap of a redundant power supply does not cause these outputs to go out of regulation in the system.

5.13.1 ISHARE

This input/output will allow two or more power supplies to share output current between them. In the case of two or more power supplies connected but with only one operating, either no AC or PS_ON high, the current share bus will meet the same requirements as a single power supply. For high line range 200VAC-240VAC, 2+0 power supplies is operating, current share accuracy is defined in Table18

Table 17 ISHARE voltage limits of each power supply

Loading (%)	ISHARE Min.	ISHARE Typ.	Max.	Unit
0%	-0.3	0	0.3	V
10%	0.6	0.8	1	V
20%	1.4	1.6	1.8	V
50%	3.8	4.0	4.2	V
100%	7.8	8.0	8.2	V

5.13.2 Sharing accuracy

Table 18 Sharing accuracy

Loading (%)	Accuracy
10%~20%	20%
20%~50%	10%
>50%	5%

5.14 Ripple / Noise

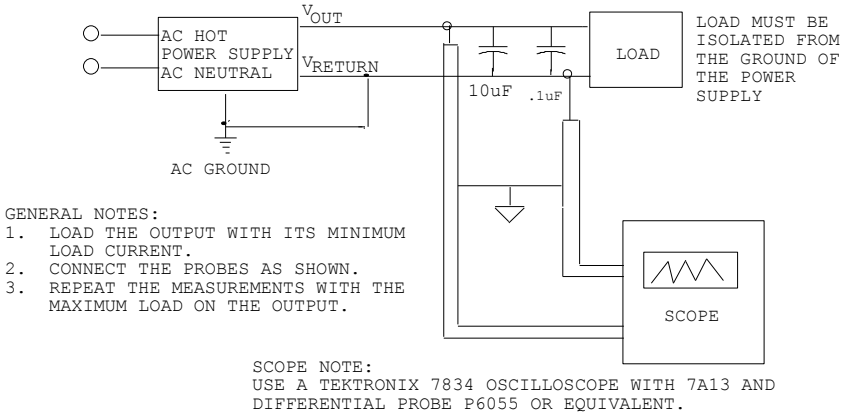
The maximum allowed ripple/noise output of the power supply is defined in following table. This is measured over a bandwidth of 10Hz to 20MHz at the power supply output connectors. A 10μF in parallel with a 0.1μF ceramic capacitor is placed at the point of measurement. To help reduce switching ripple further, an additional 2,200μF low ESR electrolytic capacitor may be placed in parallel.

Table 19 Ripples and Noise

+12V2	12VSB
120mVp-p	120mVp-p

The test set-up shall be as shown below.

Figure 1 Differential noise test setup



Note: When performing this test, the probe clips and capacitors should be located close to the load.

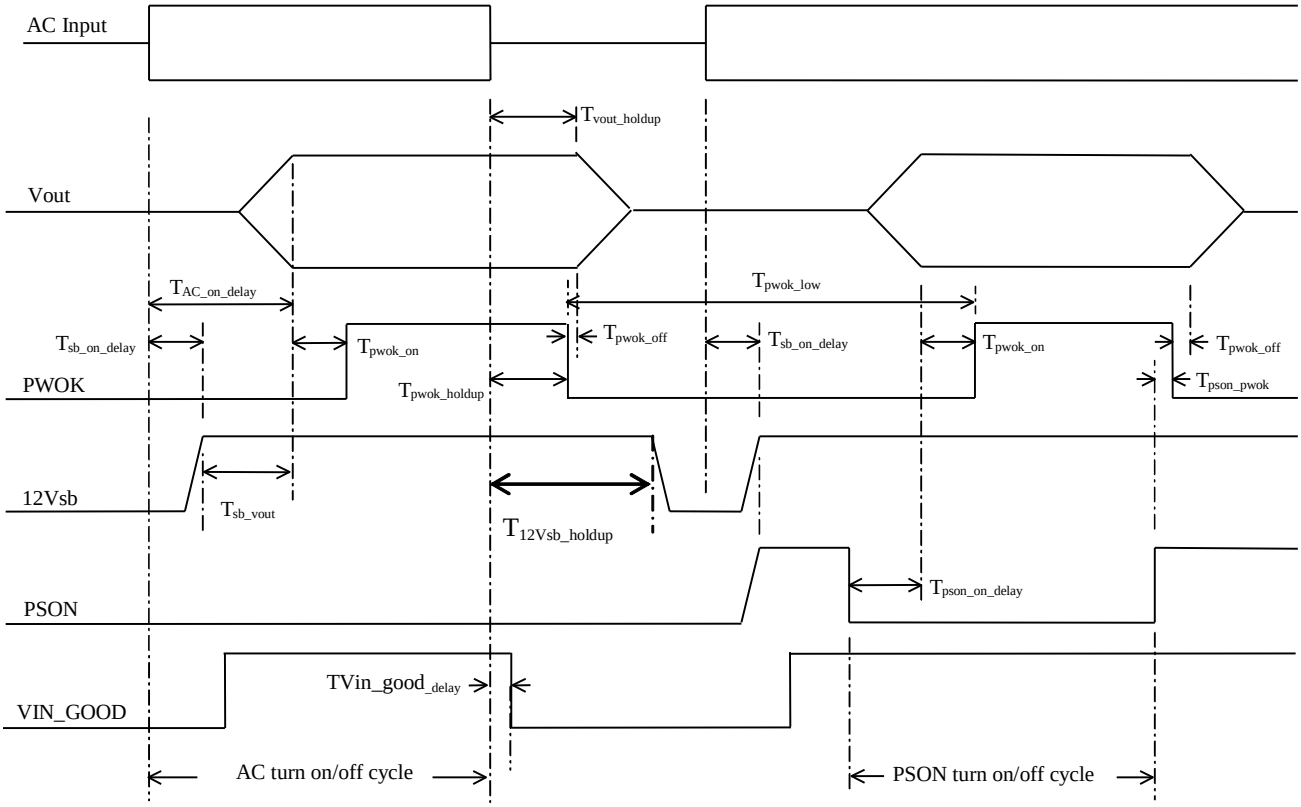
5.15 Timing requirements

These are the timing requirements for the power supply operation. The output voltages must rise from 10% to within regulation limits (T_{vout_rise}) within 5 to 70ms. For 12VSB, it is allowed to rise from 1.0 to 70ms. From 10% to 90% output voltages must rise monotonically. Table below shows the timing requirements for the power supply being turned on and off via the AC input, with PSON# held low and the PSON# signal, with the AC input applied.

Table 20 Timing requirements

ITEM	DESCRIPTION	MIN	MAX	UNITS
T_vout_rise	Output voltage rise time	5.0	70	ms
Tsb_on_delay	Delay from AC being applied to 12VSB being within regulation.		1500	ms
T ac_on_delay	Delay from AC being applied to all output voltages being within regulation.		3000	ms
Tvout_holdup	Time 12V2 output voltage stay within regulation after loss of AC	10		ms
Tpwok_holdup	Delay from loss of AC to de-assertion of PWOK	9		ms
Tpson_on_delay	Delay from PSON# active to output voltages within regulation limits.	5.0	400	ms
T pson_pwok	Delay from PSON# deactivate to PWOK being de-asserted.		50	ms
Tpwok_on	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	500	ms
T pwok_off	Delay from PWOK de-asserted to output voltages dropping out of regulation limits.	1.0		ms
Tpwok_low	Duration of PWOK being in the de-asserted state during an off/on cycle using AC or the PSON signal.	100		ms
Tsb_vout	Delay from 12VSB being in regulation to O/Ps being in regulation at AC turn on.	50	1500	ms
T12VSB_holdup	Time the 12VSB output voltage stays within regulation after loss of AC.	70		ms
TVin_good_delay	Delay from loss AC to AC_FAIL asserted.		4.0	ms

Figure 2 Turn On/Off Timing (Power Supply Signals)



6. Protection circuits

Protection circuits inside the power supply shall cause only the power supply's main outputs to shutdown. If the power supply latches off due to a protection circuit tripping, an AC cycle OFF for 15sec or a PSON# cycle HIGH for 1sec shall be able to reset the power supply.

6.1 Current limit (OCP)

The power supply shall have current limit to prevent the outputs from exceeding the values shown in table below. If the current limits are exceeded the power supply shall shutdown and latch off. The latch will be cleared by toggling the PSON# signal or by an AC power interruption. The power supply shall not be damaged from repeated power cycling in this condition. 12VSB will be auto-recovered after removing OCP limit.

Table 21 Over current protection

Output voltage	Over current limit
+12V2	110% to 130% of max output loading.
12VSB	110% to 150% of max output loading.

Table 21-1 OCP Input Condition

Parameter	OCP Input Condition	Max. Current	SMBAlert Status
+12V2	$220V_{rms}$ / $220V_{DC}$	161.5A	Low
	$200V_{rms}$ / $200V_{DC}$	145.1A	Low
	$180V_{rms}$ / $164V_{DC}$	128.7A	Low
	$100V_{rms}$	79.5A	Low
	$90V_{rms}$	71.3A	Low
12VSB	$90V_{rms}$ - $264V_{rms}$ / $164V_{DC}$ - $300V_{DC}$	2.5A	High

6.2 Over voltage protection (OVP)

The power supply over voltage protection shall be locally sensed. The power supply shall shutdown and latch off after an over voltage condition occurs. This latch shall be cleared by toggling the $PSON^{\#}$ signal or by an AC power interruption. The values are measured at the output of the power supply's connectors. The voltage shall never exceed the maximum levels when measured at the power connectors of the power supply connector during any single point of fail. The voltage shall never trip any lower than the minimum levels when measured at the power connector. 12VSB will be auto-recovered after removing OVP limit.

Table 22 Over voltage protection (OVP) limits

Output Voltage	Min.	Max.
+12V2	13V	14.5V
12VSB	13V	14.5V

6.3 Over temperature protection (OTP)

The power supply will be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an OTP condition the PSU will shutdown. OT warning SMBAlert assertion must always precede the OTP shutdown. When the power supply temperature drops to within specified limits, the power supply shall restore power automatically, while the 12VSB remains always on. The OTP circuit must have built in margin such that the power supply will not oscillate on and off due to temperature recovering condition. The OTP trip temperature level shall be at least 5°C higher than SMBAlert over temperature warning threshold level.

6.4 Input over voltage protection (OVP)

The power supply unit shall be protected against input over voltage conditions. This includes both AC and DC inputs. In an input over voltage condition the +12V2 shall shutdown. When the input drops to within safe operating limit, the power supply unit shall restart output automatically. The input OVP active levels are 300V~317V for AC input and 335V~347V for DC input, inactive levels are 283V~290V for AC input and 313V~320V for DC input.

7. Control and indicator functions

The following sections define the input and output signals from the power supply. Signals that can be defined as low true us the following convention: Signal# = low true.

7.1 PSON# input signal

The PSON# signal is required to remotely turn on/off the power supply. PSON# is an active low signal that turns on the +12V2 power rail. When this signal is not pulled low by the system, or left open, the outputs (except the 12VSB) turn off. This signal is pulled to a standby voltage by a pull-up resistor internal to the power supply.

Table 23 PSON# signal characteristics

Signal type	Accepts an open collector/drain input from the system. Pull-up to VSB located in power supply.	
PSON# = Low	ON	
PSON# = High or Open	OFF	
	Min.	Max.
Logic level low	0V	1.00V
Logic level high	2.00V	3.46V

7.2 PWOK (power ok) output signal

PWOK is a power OK signal and will be pulled HIGH by the power supply to indicate that all the outputs are within the regulation limits of the power supply. When any output voltage falls below regulation limits or when AC power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PWOK will be de-asserted to a LOW state. The start of the PWOK delay time shall inhibited as long as any power supply output is in current limit.

Table 24 PWOK signal characteristics

Signal type	Open collector/drain output from power supply. Pull-up to VSB located in the power supply	
PWOK = High	Power OK	
PWOK = Low	Power not OK	
	Min.	Max.
Logic level low	0V	0.4V
Logic level high	2.4V	3.46V
Sink current		1mA
Source current		400μA
PWOK rise and fall time		100μsec

Note: the Power Ok circuits should be compatible with 3.3V pull up resistor (>6.8k)

7.3 SMBAlert# signal

This signal indicates that the power supply is experiencing a problem that the user should investigate. This shall be asserted due to Critical events or Warning events. The signal shall activate in the case of critical component temperature reached a warning threshold, general failure, over-current, over-voltage, under-voltage, failed fan.

Table 25 SMBAlert# signal characteristics

Signal type	Open collector / drain output from power supply. Pull-up to VSB located in system.	
SMBAlert = High	OK	
SMBAlert = Low	Power alert to system	
	Min.	Max.
Logic level low	0V	0.4V
Logic level high	2.4V	3.46V
Sink current		10mA
Source current		400μA
SMBAlert# rise and fall time		100μsec

7.4 VIN_GOOD signal

VIN_GOOD is an output signal to indicate AC power is existence and is within operation range.

The VIN_GOOD should act (High to Low) within 4ms only for Vin power dropout event.

Table 26 VIN_GOOD signal characteristics

Signal type	Open collector/drain output from power supply. Pull-up to VSB located in the power supply	
VIN_GOOD= High	Vin voltage in operation range	
VIN_GOOD= Low	Vin voltage out of operation range	
	Min.	Max.
Logic level low	0V	0.4V
Logic level high	2.4V	3.46V
Sink current		1mA
Source current		400μA
VIN_GOOD rise and fall time		100μsec

7.5 PRESENT

PRESENT# is an active low output signal from the power supply used to indicate that the power supply is physically present. The design of power supply uses impedance 100 ohm to connect GND.

8. Environment requirements

8.1 Temperature

Minimum operating ambient: 0°C

Maximum operating ambient: 55°C

Non-operating ambient: -40°C to +70°C (Maximum rate of change of 20°C/hour)

8.2 Humidity

Operating: To 85% relative humidity (non-condensing)

Non-Operating: To 95% relative humidity (non-condensing)

NOTE: 95% relative humidity is achieved with a dry bulb temperature of 55°C and a wet bulb temperature of 54°C.

8.3 Altitude

Operating: 5000 m

Non-operating: 15200m

8.4 Mechanical shock

Non-operating: 50 G Trapezoidal Wave, Velocity change = 170 in. / sec.

Three drops in each of six directions are applied to each of the samples.

8.5 Random vibration

Non-operating

Sine sweep: 5Hz to 500Hz @ 0.5gRMS at 0.5 octave/min; dwell 15 min at each of 3 resonant points;

Random profile: 5Hz @ 0.01g^2/Hz to 20Hz @ 0.02g^2/Hz (slope up); 20Hz to 500Hz @ 0.02g^2/Hz (flat); Input acceleration = 3.13gRMS; 10 min. per axis for 3 axis on all samples

8.6 Thermal shock (Shipping)

Non-operating: -40°C to +70°C, 50 cycles, 30*C/min. * transition time * 15*C/min., duration of exposure to temperature extremes for each half cycle shall be 30 minutes.

9. FRU requirements

9.1 FRU data

The FRU data format shall be compliant with the IPMI ver.1.0 (per rev.1.1 from Sept.25, 1999) specification. The current version of these specifications is available at http:\\developer.intel.com/design/servers/ipmi/spec.htm. The following is the exact listing of the EEPROM content. During testing this listing shall be followed and verified.

9.2 FRU device protocol

The FRU device will implement the same protocols as the commonly used AT24C02 device, including the Byte Read, Sequential Read, Byte Write, and Page Read protocols.

9.2.1 FRU data format

The information to be contained in the FRU device follows the IPMI (Platform Management FRU Information Storage Definition) guidelines Document Revision 1.1 from November 15, 1999.

10. Firmware requirements

10.1 PMBus

Refer to “PMBus Application Profile for AC/DC & DC/DC Server Power Supplies, Revision 1.2” for the PMBus requirements. This is Intel document reference number 451620.

10.1.1 Related documents

- PMBus™ Power System Management Protocol Specification Part I – General Requirements, Transport And Electrical Interface; Revision 1.2
- PMBus™ Power System Management Protocol Specification Part II – Command Language; Revision 1.2
- System Management Bus (SMBus) Specification Version 2.0

10.1.2 Addressing

The PSU PMBus device address locations are shown below. There are two signals to set the address location of the PSU once it is installed in the system; Address1 (A1), Address0 (A0).

Table 27 PSU PMBus / FRU device address loaction

System addressing		PMBus device	FRU device
A1	A0	read / write addresses	read / write addresses
0	0	B0h / B1h	A0h / A1h
0	1	B2h / B3h	A2h / A3h
1	0	B4h / B5h	A4h / A5h
1	1	B6h / B7h	A6h /A7h

10.1.3 Hardware

The device in the power supply shall be compatible with both SMBus 2.0 ‘high power’ specification for I2C Vdd based power and drive (for Vdd = 3.3V). This bus shall operate at 3.3V.

10.1.4 PMBus power sourcing

The circuits inside the power supply shall derive their power from the standby output. For redundant power supplies the device(s) shall be powered from the system side of the or’ing device. The PMBus device shall be on whenever AC power is applied to the power supply or a parallel redundant power supply in the system.

10.1.5 Pull ups

The main pull-up resistors on SCL and SDA are provided by the system and connected to 3.3V. For the system design, the main pull-ups shall be located external to the power supply and derive their power from the standby rail.

10.1.6 Data speed

The PMBUS device in the power supply shall operate at the full 100 kbps SMBus speed and avoid using clock stretching that can slow down the bus. For example, the power supply can clock stretch while parsing a command or a power supply servicing multiple internal interrupts or NACK may require some use of clock stretching. Unsupported commands may respond with a NACK but must always set the communication error status bit in STATUS_CML.

The PMBus device shall support SMBus cumulative clock low extend time (Tlow:sext) if < 25msec. This requires the device to extend the clock time no more than 25msec between START and STOP for any given message.

10.1.7 Bus error

The PMBus device shall support SMBus clock-low timeout (Ttimeout). This capability requires the device to abort any transaction and drop off the bus if it detects the clock being held low for >25ms, and be able to respond to new transactions 10ms later.

10.1.8 New PAGE_PLUS_WRITE / PAGE_PLUS_READ commands (05h/06h)

The new PAGE_PLUS_WRITE and PAGE_PLUS_READ commands are used with the STATUS_WORD, STATUS_INPUT, STATUS_TEMPERATURE, STATUS_IOUT, and STATUS_CML to create two instances of the same command. Each instance is set by the same events but cleared by their own master in the system. The instances at PAGE 00h are controlled by the system BMC and the instances at PAGE 01h are controlled by the system ME. Below are the protocols used to read and clear the STATUS_ commands using the PAGE_PLUS_WRITE and PAGE_PLUS_READ commands.

Figure 3 Reading STATUS commands with PAGE_PLUS_READ

Reading STATUS_WORD

Block Write – Block Read Process Call with PEC

1	7	1	1	8	1	8	1	8	1		1
S	Power Supply Address	W	A	PAGE_PLUS_READ Command code	A	Byte Count=2	A	PAGE 1st instance=00h 2nd instance=01h	A	STATUS_WORD Command	A

1	7	1	1		1	8	1	8	1	8	1	1
Sr	Power Supply Address	R	A	Byte Count=2	A	STATUS_WORD Low byte	A	STATUS_WORD High byte	A	PEC	A	P

Reading STATUS_TEMPERATURE, STATUS_IOUT, STATUS_INPUT, STATUS_CML

Block Write – Block Read Process Call with PEC

1	7	1	1	8	1	8	1	8	1	8	1
S	Power Supply Address	W	A	PAGE_PLUS_READ Command code	A	Byte Count=2	A	PAGE 1st instance=00h 2nd instance=01h	A	STATUS Command	A

1	7	1	1		1	8	1	8	1	1
Sr	Power Supply Address	R	A	Byte Count=1	A	STATUS_XXX byte	A	PEC	A	P

Figure 4 Clearing STATUS commands using PAGE_PLUS_WRITE

Clearing STATUS Commands (Write ‘1’ to a clear bit)

STATUS_TEMPERATURE, STATUS_IOUT, STATUS_INPUT, STATUS_CML Block Write with PEC

1	7	1	1	8	1	8	1	8	1		1
S	Power Supply Address	W	A	PAGE_PLUS_WRITE Command code	A	Byte Count=3	A	PAGE 1st instance=00h 2nd instance=01h	A	STATUS Command	A

8	1	8	1	1
Clearing bits ‘1’=Clear	A	PEC	A	P

STATUS_WORD cannot be clear directly. It is cleared base on lower level status commands.

10.1.9 Sensors

The following PMBus commands shall be supported for the purpose of monitoring current, voltage, and power. All sensors shall continue providing real time data as long as the PMBus device is powered. This means in standby mode the main output(s) of the PSU shall be zero amps and zero volts. Sensors shall meet requirements from 100VAC to 127VAC and from 200VAC to 240VAC. They shall be tested down to 10% load.

Table 28 Current / Power / Temperature monitoring PMBus commands

PMBus command	Description
READ_EIN	New input energy counter described below. Added to PMBus rev 1.2 spec. Uses direct format for the power accumulator; unsigned integer value for the sample count.
READ_PIN	Input power meter based on PMBus rev 1.1 spec. Uses Linear formatting.
READ_IOUT	Output current in amps for the total 12V current. The other outputs are not sensed. Uses linear format.
READ_EOUT	New output energy counter described below. Added to PMBus rev 1.2 spec. Uses direct format for the power accumulator; unsigned integer value for the sample count.
READ_TEMPERATURE_1	Returns the temperature in °C of the inlet temperature. Based on PMBus rev 1.1 spec. Uses linear format.
READ_TEMPERATURE_2	Returns the temperature in °C of the hot spot temperature. Based on PMBus rev 1.1 spec. Uses linear format.

10.1.10 Sensor accuracy

The sensor commands shall meet the following accuracy requirements. The accuracies shall be met over the specified ambient temperature and the full range of rated AC input voltage.

Table 29 Accuracy requirments

PARAMETER	10% < ~ < 20%	20% ≤ ~
READ_VIN	+/-5%	+/-2%
READ_IIN	+/-5%	+/-2%
READ_PIN	+/-5%	+/-2%
READ_VOUT	+/-5%	+/-2%
READ_IOUT	+/-5%	+/-2%
READ_POUT	+/-5%	+/-2%
READ_FAN	+/-300RPM	
READ_TEMPERATURE	+/- 3ºC	

10.1.11 READ_PIN (97h)

The power supply shall provide input power data in watts. The data shall be reported using the PMBus linear format. The data shall be the average input power or filtered input power. The minimum accuracy shall be +/-2% over 20% to 100% load range; +/-5% over 10% to 19% load range. The accuracy shall be tested by polling with the READ_PIN command at a rate ranging from 1 sample / second to 10 samples / second.

Table 30 READ_PIN requirments summary

	Min.	Max.	Description
Format	PMBus linear format		Refer to PMBus specification for details.
Averaging period	2sec.	10sec.	The AC input power shall be averaged using a simple averaging method of a filtering method. This defines the max/min period for simple averaging and the bandwidth range if the filter method is used.
Filtering bandwidth	0.1Hz	0.5Hz	
Accuracy (10% to 19% load)		+/-5%	The input power shall meet requirements from 100VAC to 127VAC and from 200VAC to 240VAC.
Accuracy (20% to 100% load)		+/-2%	
System polling rate	1sample / sec.	10samples / sec.	The power supply shall be polled over this range of rates while testing accuracy.

Note: The READ_PIN power value should reset to 0W when in standby mode or when input voltage is lost.

10.1.12 READ_EIN (86h)

The new READ_EIN command is used to allow the system to apply its own input power filtering. This will allow the system to get faster input power data while preventing aliasing. The command returns an accumulated power value and an associated sample count of number of accumulated power values. This allows the system to calculate its own average power value each time the system polls the PSU.

Table 31 READ_EIN requirments summary

	Min.	Max.	Description
Format	PMBus direct format m=01h, R=00h, b=00h		Refer to PMBus specification for details.
Averaging period	=4 AC cycle		Period instantaneous AC power is averaged over to calculated Psample.
Accuracy (10% to 19% load)		+/-15%	The calculated input power shall meet requirements from 100VAC to 127VAC and from 200VAC to 240VAC.
Accuracy (20% to 100% load)		+/-5%	
System polling rate	1sample / sec.	10samples / sec.	The power supply shall be polled over this range of rates while testing accuracy.

NOTE: The READ_EIN power accumulator, roll-over counter, and sample count should keep the latest value when the power supply is put into standby mode. The power accumulator, roll-over counter and sample count should reset to 00 when AC power is lost.

10.1.13 READ_EOUT (87h)

The new READ_EOUT command is used to allow the system to apply its own output power filtering. This will allow the system to get faster output power data while preventing aliasing. The command returns an accumulated power value and an associated sample count of number of accumulated power values. This allows the system to calculate its own average power value each time the system polls the PSU.

Table 32 READ_EOUT requirments summary

	Min.	Max.	Description
Format	PMBus direct format m=01h, R=00h, b=00h		Refer to PMBus specification for details.
Averaging period	~50mS		Period instantaneous AC power is averaged over to calculated Psample.
Accuracy (10% to 19% load)		+/-15%	The calculated input power shall meet requirements from 100VAC to 127VAC and from 200VAC to 240VAC.
Accuracy (20% to 100% load)		+/-5%	
System polling rate	1sample / sec.	10samples / sec.	The power supply shall be polled over this range of rates while testing accuracy.

10.1.14 READ_EIN and READ_EOUT formats

The READ_EIN and READ_EOUT commands shall use the PMBus direct format to report an accumulated power value and the sample count. The PMBus coefficients m, R, and b shall be fixed values and the PSU shall report these values using the PMBus COEFFICIENT command. The coefficient m shall be set to 01h, coefficient R shall be set to 00h, and coefficient b shall be set to 00h.

READ_EIN and READ_EOUT shall use the SMBus Block Read with PEC protocol in the below format.

Figure 5 READ_EIN command

1	7	1	1	8	1	1	7	1	1	8	1
S	Power Supply Address	W	A	READ_EIN Command code	A	Sr	Power Supply Address	R	A	Byte Count=6	A

…

8	1	8	1	8	1	8	1	8
Accumulated power -low byte	A	Accumulated power -high byte	A	Accumulated power roll over count	A	Sample count -low byte	A	Sample count -middle byte

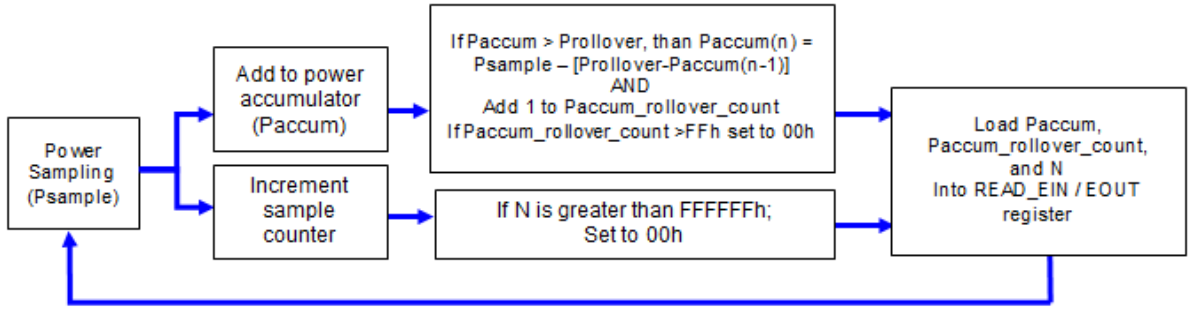
…

1	8	1	8	1	1
A	Sample count -high byte	A	PEC	A	P

READ_EIN and READ_EOUT Accumulators

The accumulated power data shall be the sum of input power values averaged over 4 AC cycles (or over 50ms for READ_EOUT). The value shall automatically roll-over when the 15 bit maximum value is reached (> 7FFFh). The sample count should increment 1 for each accumulated power value. The system shall calculate average power by dividing the accumulated power value by the sample count. The system must sample READ_EIN and READ_EOUT faster than the roll-over period to get an accurate power calculation. Below is a block diagram depicting the accumulator function in the PSU.

Figure 6 READ_EIN PSU function diagram



Psample:	The sampled power value in linear or direct format
Paccum:	2 bytes in PMBus linear or direct format. The accumulated power values made up of Psample(0) + Psample(1) + … + Psample(n)
N:	3 byte unsigned integer value. The number of accumulated power values summed in Paccum
Prollover:	The max value of Paccum before a rollover will occur
Paccum_rollover_count:	1 byte unsigned integer counting the number of times Paccum rolls over. Once this reaches FFh; it will automatically get reset to 00h

10.1.15 COFFICIENT (30h)

The power supply shall support the PMBus COEFFICIENT command. The system shall use this to read the values of m, b, and R used to determine READ_EIN and READ_EOUT accumulated power values.

Command	COEFFICIENTS support	m	B	R
READ_EIN	Yes	01h	00h	00h
READ_EOUT	Yes	01h	00h	00h
all other commands	*Optional*	*X*	*X*	*X*

10.1.16 Status commands

The following PMBus STATUS commands shall be supported. All STATUS commands except the STATUS_FAN_1_2 command shall be accessed with the new PAGE_PLUS_WRITE and PAGE_PLUS_READ commands since they are used by both the BMC and ME. The BMC and ME refer to the two instances of the commands accessed via the PAGE_PLUS_WRITE and PAGE_PLUS_READ commands. The status bits shall assert whenever the event driving the status bit is present. Once a bit is asserted it shall stay asserted until cleared using one of the methods shown in section 10.1.17. A summary of the supported STATUS commands are shown below.

The STATUS commands that are supported with the PAGE_PLUS_READ and PAGE_PLUS_WRITE commands shall still support direct access of the base STATUS_XXX commands using the read word, write word, read byte, and write byte protocols.

STATUS_FAN_1_2 command is only accessed by the system BMC. It uses the standard read byte protocol to read status and write byte protocol to clear bits.

The STATUS events are also used to control the SMBAlert# signal. The new SMBALERT_MASK command is used to define which status event controls the SMBAlert# signal. Default values for these mask bits are shown in the table below.

Table 33 PMBus status commands summary

PMBus command	Bit location	PSU state when bit is asserted ('1')	Instances PAGE00h= BMC PAGE 01h = ME	SMBALERT_MASK defaults 0=causes assertion of SMBAlert# 1=does not causes assertion of SMBAlert#
STATUS_BYTE			00h, 01h	
OFF	6 (lower)	OFF		NA
VOUT_OV	5 (lower)	Refer to STATUS_VOUT		NA
IOUT_OC_FAULT	4 (lower)	Refer to STATUS_IOUT		NA
VIN_UV_FAULT	3 (lower)	Refer to STATUS_INPUT		NA
TEMPERATURE	2 (lower)	Refer to STATUS_TEMPERATURE		NA
CML	1 (lower)	Refer to STATUS_CML		NA
STATUS_WORD			00h, 01h	
OFF	6 (lower)	OFF		NA
VOUT_OV	5 (lower)	Refer to STATUS_VOUT		NA
IOUT_OC_FAULT	4 (lower)	Refer to STATUS_IOUT		NA
VIN_UV_FAULT	3 (lower)	Refer to STATUS_INPUT		NA
TEMPERATURE	2 (lower)	Refer to STATUS_TEMPERATURE		NA
CML	1 (lower)	Refer to STATUS_CML		NA
VOUT	7 (upper)	Refer to STATUS_VOUT		NA
IOUT/POUT	6 (upper)	Refer to STATUS_IOUT		NA
INPUT	5 (upper)	Refer to STATUS_INPUT		NA
PWR_ GOOD	3 (upper)			1
FANS	2 (upper)	Refer to STATUS_FAN		NA 1
STATUS_VOUT			NA	
VOUT_OV_FAULT	7	OFF		1,
VOUT_UV_FAULT	4	OFF		1,
STATUS_IOUT			00h, 01h	
IOUT_OC_FAULT	7	OFF		1
IOUT_OC_WARNING	5	ON		Page 00h =1, Page 01h =0
POUT_OP_FAULT	1	OFF		1
POUT_OP_WARNING	0	ON		1
STATUS_INPUT			00h, 01h	
VIN_OV_FAULT	7	OFF		1
VIN_UV_WARNING	5	ON		1
VIN_UV_FAULT [1]	4	OFF		Page 00h =1, Page 01h =0
Unit off for low input voltage	3	OFF		1
IIN_OC_WARNING	1	ON		1
PIN_OP_WARNING	0	ON		1
STATUS_TEMPERATURE			00h, 01h	
OT_FAULT	7	OFF		1
OT_WARNING	6	ON		Page 00h =1, Page 01h =0
STATUS_FANS_1_2			00h	
Fan 1 fault	7	OFF		1
Fan 1 warning	5	ON		1
STATUS_CML			00h, 01h	
CMD_FAULT	7	ON		1

DATA_FAULT	6	ON		1
PEC_FAULT	5	ON		1

10.1.17 Resetting of Status bits

The STATUS_ commands shall be reset only by the below methods. If the event is still present that caused the assertion of the status bit; the bit shall re-assert after clearing.

- Writing a '1' to any given bit location shall reset only that bit of the command.
- Sending a CLEAR_FAULTS command to the power supply shall reset all STATUS_ bits to '0'.
- The STATUS commands accessed via the PAGE_PLUS_READ command shall not be effected by CLEAR_FAULTS.
- Cycling AC power OFF then ON shall reset all STATUS_ bits to '0'.
- Systems with redundant power supplies where only one of the supplies cycle AC power OFF/ON; the power cycled power supply shall reset the STATUS_ bits to '0' only when powered back ON. If the power supply is kept OFF, the STATUS_ bits shall not be reset.
- Cycling the PSON# signal from de-asserted to asserted shall reset the STATUS_ bits to '0'. The bits shall be reset only on the assertion of PSON#; not the de-assertion.

NOTE. Setting a PAGE value of FFh is used to clear all status bits in all PAGEs with the CLEAR_FAULT command.

10.1.18 Default Limits for warning and faults

Warning limits shall be set with enough margin to guarantee no false warnings will occur is power supply operates within the specified requirements, but before the power supply shuts down. Fault limits shall be set at limits equal to or greater than the level at which the power supply shuts down.

10.1.19 Resetting to default limits

The power supply shall reset the warning and fault limits to default values for the following case.

- AC power cycling
- PSON power cycling
- PSU would reset the VIN_UV_FAULT and VIN_UV_WARNING flags when AC recovery

10.1.20 Faults and Error Checking

The PSU shall support PEC per the SMBus 2.0 specification.

10.1.21 Packing error Checking

The PSU shall support packet error checking to support error checking and handling.

10.1.22 Capability and inventory reporting

The follow commands shall be supported for discovery of the power supplies capabilities.

Table 34 PMBus PSU Capability & Inventory Commands Summary

PMBus command	Value	Description
CAPABILITY	PEC = supported Bus speed = 100kHz SMBAlert# = supported	Defines the power supplies PEC support, bus speed, and support of SMBAlert
QUERY	Linear formats for all but READ_EIN / READ_EOUT which is Direct	Used to determine if the PSU supports a specific command.
PMBUS_REVISION	0010 0010	Used to verify the PMBUS_REVISION the PSU is based on. This shall be set to revision 1.2.
MFR_TEMP1_MAX	Trip threshold for the ambient temperature sensor (TEMP1) to assert SMBAlert#	Defines the maximum inlet temperature to generate a warning condition in the STATUS_TEMPERATURE command.
MFR_TEMP2_MAX	Trip threshold for the hot spot temperature sensor (TEMP2) to assert SMBAlert#	Defines the maximum hotspot temperature to generate a warning condition in the STATUS_TEMPERATURE command.
MFR_IOUT_MAX	Rated output current using the linear format	Defines the maximum rated output current on the 12V2 rail.
MFR_POUT_MAX	Rated output power using the linear format	Defines the maximum rated output power of the PSU.
APP_PROFILE_SUPPORT	05h	Defines that the PSU supports this application profile.

10.1.23 SMBAlert#

The SMBAlert# signal may be asserted by the PSU for any of the supported STATUS events. The events that control SMBAlert# can be masked using the SMBALERT_MASK command. Default masking is shown in section “Status commands” .

10.1.24 SMBAlert# operation in standby mode

The PSU shall assert the SMBAlert# signal only when the main outputs are ON. SMBAlert# shall stay de-asserted when the PSU is in standby mode when any bits in the STATUS commands get asserted.

10.1.25 Continuous assertion after clearing if condition is still present

If the warning or fault condition is present when a bit is cleared, the bit and associated SMABLERT# signal stays asserted with no momentary transition to a de-asserted state.

10.1.26 SMBalert# mask (1Bh)

This allows the system to mask events from asserting the SMBAlert# signal and to read back this information from the PSU. SMBALERT_MASK command can be used with any of the supported STATUS events. The events are masked from asserting SMBAlert# by writing a ‘1’ to the associated STATUS bits. The SMBALERT_MASK command is used in conjunction with the PAGE_PLUS command and STATUS_ commands. Below are the protocols.

Figure 7 PAGE_PLUS_READ command

Reading mask value using PAGE_PLUSE Block Write – Block Read Process with PEC

1	7	1	1	8	1	8	1	8	1	8
S	Power Supply Address	W	A	PAGE_PLUSE_READ Command code	A	Byte Count=3	A	PAGE 1st instance=00h 2nd instance=01h	A	SMBALERT_MASK Command code

1	8	1	1	7	1	1	8	1	8	1	8	1	1
A	STATUS Command	A	Sr	Power Supply Address	R	A	Byte Count=1	A	Mask values 1=masked	A	PEC	A	P

Figure 8 PAGE_PLUS_WRITE command

Writing mask value using PAGE_PLUSE Block Write Process with PEC

1	7	1	1	8	1	8	1	8	1	8
S	Power Supply Address	W	A	PAGE_PLUSE_WRITE Command code	A	Byte Count=4	A	PAGE 1st instance=00h 2nd instance=01h	A	SMBALERT_MASK Command code

1	8	1	8	1	8	1	1
A	STATUS Command	A	Mask values 1=masked	A	PEC	A	P

STATUS_WORD is not used with SMBALERT_MASK. Only the 'root' event bits are used to control the SMBAlert# signal.

10.1.27 Alert Response Address (ARA)

The PSU shall not support ARA. After asserting the SMBAlert# signal the PSU shall keep its address at it standard address; not change to 18h.

10.1.28 Setting and Resetting the SMBAlert# signal

The SMBAlert# signal shall be asserted whenever any un-masked event has occurred. This is a level detected event. Whenever the event is present SMBAlert# shall be asserted. If the SMBAlert# signal is cleared; it shall be immediately re-asserted if the an event is still present.

The SMBAlert# signal shall be cleared and re-armed by the following methods.

- Clearing STATUS bits causing the asserted SMBAlert# signal.
- Power cycling with PSON or with AC power

10.1.29 Fan speed control

The PSU shall support the PMBus commands to allow the system to control and monitor the PSU's fan.

10.1.30 FAN_CONFIG_1_2 (3Ah)

The FAN_CONFIG_1_2 command is used to define the presence of a fan and the method it is controlled (by duty cycle or RPM).

Table 35 FAN_CONFIG_1_2 Command

Bits	Value	Meaning
7	1	Fan in position 1
6	0	Fan 1 commanded in Duty Cycle(Percentage)
5:4	Not used	
3	0	No fan in position 2
2	Not used	
1:0	Not used	

10.1.31 FAN_COMMAND_1 (3Bh)

The system may increase the power supplies fan speed through using the FAN_COMMAND_1 command. This command can only increase the power supplies fan speed; it cannot decrease the PSU fan speed below what the PSU commands.

The control is configured to be duty cycle controlled using the linear format of the PMBus protocol.

The exponent N is fixed to a value of 0 (N = 0).

10.1.32 READ_FAN_SPEED_1 (90h)

The system will read the fan speed by using the READ_FAN_SPEED_1 command. This data shall return the fan speed in the PMBus linear format.

10.1.33 PSU commands supported for testing purposes

The PSU shall support the following (optional but recommended) commands for PSU testing purposes only.

10.1.34 IOUT_OC_WARN_LIMIT (4Ah)

The IOUT_OC_WARN_LIMIT command sets the value of the output current that causes an output over-current warning. The two data bytes are formatted in the Linear Data format.

10.1.35 OT_WARN_LIMIT (51h)

The power supply shall allow the system to set new values to the warning threshold for the hot spot temperature sensor using the READ_TEMPERATURE_2 command. This will be used by the system to simulate an assertion of the SMBAlert# signal due to a temperature warning event. This value shall be reset to the default value of any AC power cycle or PSON power cycle.

10.1.36 IIN_OC_WARN_LIMIT (5Dh)

The IIN_OC_WARN_LIMIT command sets the value of the input current, in amperes, that causes a warning that the input current is high. The two data bytes are formatted in the Linear Data format.

10.1.37 POUT_OP_WARN_LIMIT (6Ah)

The POUT_OP_WARN_LIMIT command sets the value of the output power, in watts, that causes a warning that the output power is high. The two data bytes are formatted in the Linear Data format.

10.1.38 PIN_OP_WARN_LIMIT (6Bh)

The PIN_OP_WARN_LIMIT command sets the value of the input power, in watts, that causes a warning that the input power is high. The two data bytes are formatted in the Linear Data format.

10.2 Cold Redundant requirements

In 1+1 redundant power system, the CR pins shall be connected together at user system board for Cold Redundant function.

For AC power input and 1+1 redundant power system, the Cold Redundant function is enabled via PMBUS to set the one unit in MASTER mode and another in SLAVE mode.

The unit with SLAVE mode shall be in sleep mode (+12V2 stop the power out) for ISHARE < 1.52V(38% x 8V x 1/2, 38% full of load with parallel). The unit with SLAVE mode shall recover the power out for ISHARE > 6.56V(82% x 8V, 82% of full load).

The power supply unit consumption is below 5W in SLEEP mode. When one of two PSUs is out of order, the other PSU can take over the output power automatically.

DC OFF LINE FUNCTION

In 1+1 power system, the CR pins shall be connected together at user system board for DC OFF LINE function.

For 1+1 power system, one unit is with AC power input and another is with DC power input, the OFF LINE FUNCTION is enabled via PMBUS.

The power supply unit with DC power input can be set in SLAVE mode.

The power supply unit shall be in sleep mode (+12V2 & 12VSB stop the power out) with DC input and SLAVE mode. The power supply unit consumption is below 5W in SLEEP mode.

11. Summary of PMBus commands

CMD Code	CMD name	SMBus Transient type	Data bytes length	Format	Value range	Power On default value
00h	PAGE	R/W byte	1	hex integer	0x00, 0x01, 0xFF	0x00
03h	CLEAR_FAULTS	Send byte	0	n/a	n/a	n/a
05h	PAGE_PLUS_WRITE	Write block				
06h	PAGE_PLUS_READ	Block Write-Block Read Process Call				
19h	CAPABILITY	Read byte	1	bit file	n/a	90h
1Ah	QUERY	Block Write-Block Read Process Call	1	bit file	n/a	n/a
1Bh	SMBALER_MASK	Write Word/Block Write-Block Read Process Call	2	hex integer		
30h	COEFFICIENT	Block Write-Block Read Process Call	5	hex integer		
3Ah	FAN_CONFIG_1_2	Read byte	1	bit file	00h-FFh	80h
3Bh	FAN_COMMAND_1	R/W word	2	linear-11	0-100	0
4Ah	IOUT_OC_WARN_LIMLT	R/W word	2	linear-11		185.5
51h	OT_WARN_LIMIT	R/W word	2	linear-11		110
5Dh	IIN_OC_WARN_LIMIT	R/W word	2	linear-11		12
6Ah	POUT_OP_WARN_LIMLT	R/W word	2	linear-11		2300
6Bh	PIN_OP_WARN_LIMIT	R/W word	2	linear-11		2640
78h	STATUS_BYTE	Read byte	1	bit file	n/a	00h
79h	STATUS_WORD	Read word	2	bit file	n/a	0000h
7Ah	STATUS_VOUT	Read byte	1	bit file	n/a	00h
7Bh	STATUS_IOUT	Read byte	1	bit file	n/a	00h
7Ch	STATUS_INPUT	Read byte	1	bit file	n/a	00h
7Dh	STATUS_TEMPERATURE	Read byte	1	bit file	n/a	00h
7Eh	STATUS_CML	Read byte	1	bit file	n/a	00h
81h	STATUS_FANS_1_2	Read byte	1	bit file	n/a	00h
86h	READ_EIN	Read block	5	direct		n/a
87h	READ_EOUT	Read block	5	direct		n/a
88h	READ_VIN	Read word	2	linear-11	0<x<=512	n/a
89h	READ_IIN	Read word	2	linear-11	0<x<=32	n/a
8Bh	READ_VOUT	Read word	2	linear-16	0<x<=16	n/a
8Ch	READ_IOUT	Read word	2	linear-11	0<x<=256	n/a
8Dh	READ_TEMPERATURE1 (Ambient)	Read word	2	linear-11		n/a
8Eh	READ_TEMPERATURE2 (Secondary Hotspot)	Read word	2	linear-11		n/a
8Fh	READ_TEMPERATURE3 (Primary Hotspot)	Read word	2	linear-11		n/a
90h	READ_FAN_SPEED_1	Read word	2	linear-11	0<x<=32768	n/a
96h	READ_POUT	Read word	2	linear-11	0<x<=2048	n/a
97h	READ_PIN	Read word	2	linear-11	0<x<=4096	n/a
98h	PMBUS_REVISION	Read byte	1	bit file	n/a	22h
99h	MFR_ID	Read block	13	ASCII	n/a	Seasonic POWER
9Ah	MFR_MODEL	Read block	12	ASCII	n/a	TBD

9Bh	MFR_REVISION	Read block	3	ASCII	n/a	XXX
9Ch	MFR_LOCATION	Read block	5	ASCII	n/a	CHINA
9Dh	MFR_DATE	Read block	4	ASCII	n/a	n/a
9Eh	MFR_SERIAL	Read block	16	ASCII	n/a	n/a
9Fh	APP_PROFILE_SUPPORT	Read byte	1	hex integer	n/a	05h
A0h	MFR_VIN_MIN	Read word	2	linear-11	n/a	90
A1h	MFR_VIN_MAX	Read word	2	linear-11	n/a	264
A2h	MFR_IIN_MAX	Read word	2	linear-11	n/a	10
A3h	MFR_PIN_MAX	Read word	2	linear-11	n/a	2200
A4h	MFR_VOUT_MIN	Read word	2	linear-16	n/a	11.59
A5h	MFR_VOUT_MAX	Read word	2	linear-16	n/a	12.81
A6h	MFR_IOUT_MAX	Read word	2	linear-11	n/a	161.5
A7h	MFR_POUT_MAX	Read word	2	linear-11	n/a	2000
A8h	MFR_TAMBIENT_MAX	Read word	2	linear-11	n/a	55
A9h	MFR_TAMBIENT_MIN	Read word	2	linear-11	n/a	0
ABh	MFR_EFFICIENCY_HL	Read block	14	linear-11	n/a	
C0h	MFR_MAX_TEMP_1(Ambient)	Read word	2	linear-11	n/a	65
C1h	MFR_MAX_TEMP_2 (Secondary Hotspot)	Read word	2	linear-11	n/a	110
C2h	MFR_MAX_TEMP_3 (Primary Hotspot)	Read word	2	linear-11	n/a	110
D0h	MFR_COLD_REDUNDANCY_ CONFIG	R/W byte	1	bit file	00h-02h	00h
D9h	MFR_FW_REVISION	Read block	3			

12. Reliability

12.1 Component de-rating

Component de-rating followed Seasonic Component de-rating guideline.

12.2 Life requirement

The power supply shall support 5 years MIN. calculated for: 60% of max continues load @ 35°C ambient temperature and @ 230VAC line voltage.

12.3 Mean time between failure (MTBF)

The power supply shall have a minimum MTBF of 250,000 hours at 75% load,40°C continuous loading, using the Telcordia SR-332 issue 2 prediction method. Or 250,000 hours demonstrated at 75% load and 40°C.

13. Regulatory requirements

Intended Application – This product was evaluated as Information Technology Equipment (ITE), which may be installed in offices, schools, computer rooms, and similar commercial type locations. The suitability of this product for other product categories and environments (such as: medical, industrial, telecommunications, NEBS, residential, alarm systems, test equipment, etc.), other than an ITE application, may require further evaluation.

13.1 Product Safety compliance

UL62368-1/CSA 62368-1 (USA / Canada)

EN62368-1 (Europe)

IEC60950-1 (International)

IEC62368-1

CB Certificate & Report, IEC60950-1 (report to include all country national deviations)

Nordics – EMKO-TSE (74-SEC) 207/94

CE - Low Voltage Directive 2006/95/EC (Europe)

GB4943- CNCA Certification (China)

13.2 Product EMC compliance – Class A compliance

Note: The product is required to comply with Class A emission requirements as the end system that it is configured into is intended for a commercial environment and market place. Power supply is to have minimum of 6db margin to Class A.

FCC /ICES-003 - Emissions (USA/Canada) Verification

CISPR 32 – Emissions (International)

EN55032 - Emissions (Europe)

EN55024 - Immunity (Europe)

- EN61000-4-2 Electrostatic Discharge
- EN61000-4-3 Radiated RFI Immunity
- EN61000-4-4 Electrical Fast Transients
- EN61000-4-5 Electrical Surge
- EN61000-4-6 RF Conducted
- EN61000-4-8 Power Frequency Magnetic Fields
- EN61000-4-11 Voltage Dips and Interruptions

*EN61000-3-2 - Harmonics (Europe)

*EN61000-3-3 - Voltage Flicker (Europe)

CE – EMC Directive 89/336/EEC (Europe)

JEIDA (Japan)

AS/NZS CISPR 32 (Australia / New Zealand)

GB 9254 – (EMC) Certification (China)

GB 17625.1 - (Harmonics) CNCA Certification (China)

13.3 Certification / Registrations / Declarations

UL Certification (US/Canada)

CB Certificate & Report

CE Declaration of Conformity (CENELEC Europe)

CCC Certification (China)

BSMI Certification (Taiwan)

Notes:

- Certification shall be done to the most recent standard editions.
- To support ALPHA or BETA development power supply shipments, at least one 3rd party certification is required (e.g. TUV, UL, etc.).
- Power Supply Vendor requires providing copy of each certification.

14. List of banned substances

The environment related substances listing in Seasonic DOC no. HPT-01-043 is forbidden. Used in product, part and manufacturing process.