規格書 SPECIFICATION

品名

REDUNDANT SWITCHING POWER SUPPLY

STYLE NAME:

型號

DR1S2-5300V4V

MODEL NO.:

料號

PART NO.:

版次

A1

REVISION:

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新巨企業股份有限公司 電源事業處 ZIPPY TECHNOLOGY CORP. POWER DIVISION

Revision

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1.0 Scope

This specification defines the performance characteristics of a grounded > 300 watts, 5 output level power supply. This specification also defines world wide safety requirements and manufactures process test requirements.

DR1S2-5300V4V power system is a 1+1 Redundant power system consisting of two DP1S-2300V-R power modules and one DR1S2-5300V4V power system frame.

2.0 Input requirements

2.1 Voltage (sinusoidal)

 $-36 \sim -72 \text{ VDC}$ Range Nomal - 48VDC

2.2 Steady-state current

 $-36 \sim -72 \text{ VDC} / 12 \sim 6 \text{ amp } (9 \text{ amp at } -48 \text{VDC})$

2.3 Inrush current

70 amps @- 48VDC (at 25 degrees ambient cold start)

3.0 Output requirements

3.1 DC load requirements

Normal	Load current		Regulation tolerance		
Output voltage	Max.1+1	Min 1+1	Max.	Min.	
+5V	20	0.5	+5%	-5%	
+12V	24	2.0	+5%	-5%	
-12V	0.5	0.1	+10%	-10%	
+3.3V	20	0.5	÷5%	-5%	
÷5VSB	2.5	0.1	+5%	-5%	

^{*** +5}V and +3.3V total output max : 140W ***

When doing the cross regulation test(one output channel at high load and the other output channels at low load), it is requested to set the higher output channel at 80% max. of its spec., and the lower output channels at 20% max, of theirs.

3.2 Regulation

Output DC	Line
voltage	regulation
+5V	±50mV
÷12V	$\pm 120 mV$
-12V	±120mV
+3.3V	±50mV
+5VSB	±50mV

^{***} Total output max : 300W ***

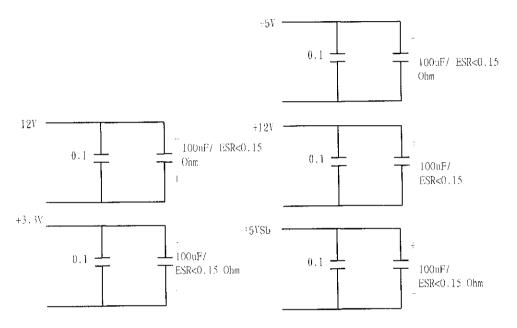
^{***} When conditions of both $\pm 5V/0A \& \pm 3.3V/0A$, min load of 4A at $\pm 12V$ is a must.

3.3 Ripple and noise

3.3.1 Specification

15V	50mV (P-P)
+12V	120mV (P-P)
-12V	120mV (P-P)
±3.3V	50mV (P-P)
⊬5VSB	50mV (P-P)

3.3.2 Ripple voltage test circuit



0.1uf is ceramic, the other is electrolytic capacitor. Noise bandwidth is from DC to 20Mhz

3.4 Overshoot

Any overshoot at turn on or turn off shall be less than 10% of the nominal voltage value, all output shall be within the regulation limit of section 3.1 before issuing the power good signal of section 6.0.

3.5 Efficiency

Power supply efficiency >80% at -48V, full load.

NOTE:

Any difference either on the DC output cable (i.e., length, wire gauge) or on the accurate of instruments will conclude different test result.

3.6 Remote on/off control

The power supply DC outputs (with the exception of +5VSB) shall be enabled with an active-low, TTL-compatible signal("PS-ON") When PS-ON is pulled to TTL low, the DC outputs are to be enabled. When PS-ON is pulled to TTL high or open circuited, the DC outputs are to be disabled.

4.0 Protection

4.1 Input (primary)

The input power line must have an over power protection device in accordance with safety requirement of section 8.0

4.2 Output (secondary)

4.2.1 Over power protection (one unit)

The power supply shall provide over power protection on the power supply latches all DC output into a shutdown state. Over power of this type shall cause no damage to power supply after over load is removed and a power on/off cycle is initiated, the power supply will restart. Trip point total power min. 110%, max. 160%.

4.2.2 Over voltage protection

If an over voltage fault occurs, the power supply will latch all DC output into a shutdown state before

 $+5V : 5.6V \sim 6.7V$ $+3.3V : 3.6V \sim 5V$ $+12V : 13.0V \sim 17.0V$

4.2.3 Short circuit

- A: A short circuit placed on any DC output to DC return shall cause no damage.
- B: The power supply shall be latched in case any short circuit is taken place at +5V, +3.3V, +12V, -12V output.
- C: The power supply shall be auto-recovered in case any short circuit is taken place at +5VSB.

5.0 Power supply sequencing

5.1 Power on (see fig.1)

5.2 Hold up time

When power shutdown DC output 5V must be maintain 1.6msec in regulation limit at normal input voltage.

5.3 Power off sequence (see fig. 1)

6.0 Signal requirements

6.1 Power good signal (see fig. 1)

The power supply shall provide a "power good" signal to reset system logic , indicate proper operation of the power supply , and give advance warning of impending loss of regulation at turn off. This signal shall be a TTL compatible up level (2.4V to 5.25V) when +5V output voltage are present and above the minimum UV sense levels specified in paragraph 6.2 , or a down level (0.0V to 0.8V) when any output is below its minimum UV sense level.

At power on , the power good signal shall have a turn on delay of at least 100ms but not greater than 500ms after the output voltages have reached their respective minimum sense levels.

7.0 Environment

7.1 Temperature

Operating temperature Storage temperature

Safety regulation temperature

0 to 50 degrees centigrade -20 to 80 degrees centigrade

Applied at room temperature (25°C)

7.2 Humidity

Operating humidity Non-operating humidity 20% to 80% 10% to 90%

7.3 Insulation resistance

Primary to secondary

: 20 meg. ohm min. 500 VDC : 20 meg. ohm min. 500 VDC Primary to FG

7.4 Dielectric withstanding voltage

For approval purpose:

Primary to secondary Primary to FG

: 3KVAC for 1min. : 1500 VAC for 1 min.

For production purpose:

Primary to FG

: 1500VAC for 1 sec

8.0 Safety

8.1 Underwriters laboratory (UL).

The power supply designed to meet UL 60950.

8.2 Canadian standards association (CUL)

The power supply designed to meet CSA C22.2 No. 60950.

8.3 TUV

The power supply shall be designed to meet TUV EN-60950.

8.4 CCC Standards

The power supply shall be designed to meet GB9254-2008, GB4943-2001. GB17625.1-2003.

9.0 Reliability

9.1 Burn in

All products shipped to customer must be processed by burn-in. The burn- in shall be performed for 1 hour at full load.

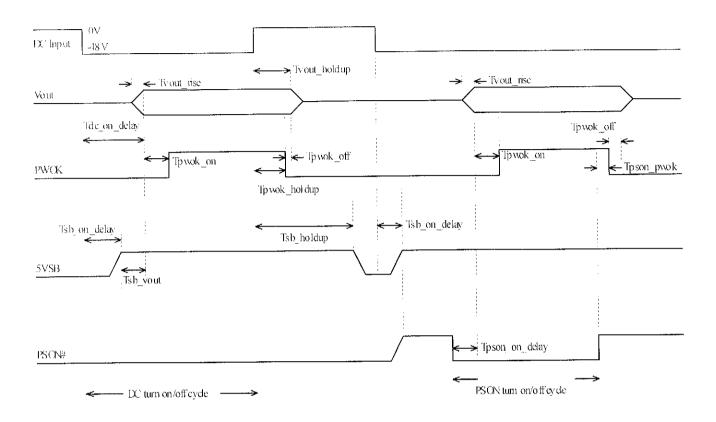
10.0 Mechanical requirements

Physical dimension: 207 mm * 85 mm * 84 mm (D*W*H)

11.0 Warning method

- 11.1 Audio alarm(buzzer sound,resetable)
- 11.2 Fault LED
- 11.3 Power defective signal delivery(TTL.Lowactive)

12.0 Output voltage Timing



Item	Description	MIN	MAX	UNITS
Tsb on delay	Delay from DC being applied to 5VSB being		3500	ms
 "	within regulation.			
Tdc_on_delay	Delay from DC being applied to all output		4500	ms
	voltages being within regulation.			
Tvout holdup	Time all output voltages stay within regulation	1.6		ms
	after loss of DC.			<u> </u>
Tpwok_holdup	Delay from loss of DC to deassertion of PWOK.	0.6		ms
Tpson on_delay	Delay from PSON# active to output voltages	5	400	ms
	within regulation limits.			
Tpson_pwok	Delay from PSON# deactive to PWOK being		50	ms
	deasserted.			
Tpwok on	Delay from output voltages within regulation	100	500	ms
	limits to PWOK asserted at turn on.			
Tpwok off	Delay from PWOK deasserted to output	1		ms
	voltages (3.3V, 5V, 12V, -12V) dropping out of			
	regulation limits.			
Tsb vout	Delay from 5VSB being in regulation to O/Ps	5	1000	ms
	being in regulation at DC turn on.			
Tsb holdup	Time 5VSB output voltage stays within	1		ms
ordill "	regulation after loss of DC.			
Tvout rise	Output voltage rise time from each main output.		50	ms

《Figure 1》